CLAIMS:

1. An amplifier circuit for amplifying an input signal and having a conduction angle of at least about 180°, said amplifier circuit comprising an amplifying transistor and a dc bias circuit for biasing said amplifying transistor to obtain said conduction angle, said dc bias circuit having a self-bias boosting circuit comprising a Wilson current-mirror integrated with a cascode current-mirror circuit to form an extended Wilson current -mirror circuit having an output coupled to a control terminal of said amplifying transistor by a resistor, and a capacitor coupled from said extended Wilson current-mirror circuit to a common terminal.

2. An amplifier circuit as in claim 1, wherein said amplifier circuit is a Class AB amplifier circuit.

3. An amplifier circuit as in claim 1, wherein said cascode current-mirror circuit comprises a first pair of transistors having main current paths connected in series, said output being taken from a common point of said series connection, and a second pair of transistors having main current paths connected in series, with a bias current source being coupled from a power supply terminal of the amplifier to a control electrode of a first transistor of said first pair of transistors and to a control electrode of a first transistor of said second pair of transistors.

4. An amplifier circuit as claimed in claim 3, further comprising a resistor coupled in series with and between said second pair of transistors.

5. An amplifier circuit as in claim 4, wherein a second transistor of said first pair and a second transistor of said second pair each have a main current path connected to said common terminal.

6. An amplifier circuit as in claim 5, further comprising a further transistor forming a part of said Wilson current mirror circuit and having a control electrode coupled to a control electrode of said second transistor of said first pair and a control electrode of said

second transistor of said second pair, and having a main current path coupled between said common terminal and a control electrode of both said first transistor of said first pair and said first transistor of said second pair at a first junction.